UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,473	02/23/2005	Peter Bode	DE 020198	3287

65913 7590 10/25/2007

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
PEREZ, JAMES M	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
10/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,473	BODE ET AL.	
	Examiner	Art Unit	
	James M. Perez	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/21/2005 and 11/09/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claim Objections

1. Claims 1-5, and 7-8 are objected to because of the following informalities:

(1) Claims 1-6 must set forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation, 37 CFR1.75(i).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4,6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vankka (A GSM/EDGE/WCMDA Modulator With On-Chip D/A Converter for Base Stations) in view of Fischer (US 2003/0160654).

With regards to claims 1 and 7, Vankka teaches a modulator (**fig. 1**) and signal processing method (**fig. 1**)

means for generating a digital I/Q signal (**fig. 1: Section 2A: paragraph 2**) having a plurality of time-slots (**Section 3: paragraph 2**), and

digital ramp generator and output power level controller which allows power ramping on a time-slot basis (**Section 3**).

Vankka remains silent with respect to teaching the modulator explicitly teaching introducing a dip in an envelope in a guard interval between adjacent time-slots.

Fischer teaches the modulator comprising:

means for introducing a dip in an envelope (**fig. 2: paragraphs 13 and 27-29**) in a guard interval between adjacent time-slots (**fig. 2: paragraphs 13 and 27-29**).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the I/Q modulation circuit of Vankka with the I/Q transmitting apparatus of Fischer in order to create an enhanced transmission system which reduces the mean power loss in a system using different modulation methods, such as GMSK and 8PSK (**Fischer: paragraphs 6 and 8**).

With regards to claims 2 and 8, Vankka in view of Fischer teaches the modulator of claim 1 and method of claim 7.

Vankka further teaches the modulator further comprising:

a means for generating a digital I/Q signal having a plurality of time-slots (**disclosed in claim 1 and claim 7**); and

a digital multiplier (**fig. 1: digital multiplier**) for multiplying the I signal and the Q signal of the I/Q signal with a waveform (**fig. 1: ramp generator, power level controller and multiplier: note dip-shaped waveform is disclosed in claim 1 and claim 7**).

Vankka is silent with respect to teaching the modulator wherein the means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between

adjacent time-slots comprises: introducing the I signal and the Q signal of the I/Q signal with a dip-shaped waveform.

Fischer teaches the modulator wherein

the means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots of the plurality of time-slots (**disclosed in claim 1 and claim 7**) comprises:

means for introducing the I signal and the Q signal of the I/Q signal with a dip-shaped waveform (**fig. 2: t2 and t3: fig. 2: paragraphs 13 and 27-29**).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the digital I/Q modulation circuit including the digital multiplier and ramp generator of Vankka with the means for introducing a dip-waveform to an I/Q signal disclosed in Fischer in order to create an enhanced transmission system which reduces the mean power loss in a system using different modulation methods, such as GMSK and 8PSK (**Fischer: paragraphs 6 and 8**).

With regards to claims 3 and 9, Vankka in view of Fischer teaches the modulator of claim 1 and method of claim 7.

Vankka further teaches the modulator further comprising:

a pulse shaping filter (**fig. 1: ramp generator and power level controller, and pulse shaping filters**)

Vankka is silent with respect to teaching a pulse shaping filter with means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between

adjacent time-slots comprising: means for generating a step-off response followed by a step-on response of the pulse shaping filter.

Fischer teaches a pulse shaping filter (**fig. 1: elements 20, 90, and 100**) with means for introducing the dip in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots (**disclosed in claim 1 and claim 7**) comprising:

means for generating a step-off response followed by a step-on response (**fig. 2: t2 and t3: paragraphs 13 and 27-29**) of the pulse-shaping filter (**fig. 1: elements 20, 90, and 100: paragraphs 13 and 27-29**).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the modulation circuit including the ramp generator, power level controller, and pulse shaping filters of Vankka with the pulse shaping filter with the mean for generating a step-off response followed by a step-on response in order to create an enhanced transmission system which reduces the mean power loss in a system using different modulation methods, such as GMSK and 8PSK (**Fischer: paragraphs 6 and 8**) and provide a smooth transition in the guard periods between successive time slots when switching between different modulation schemes (**Fischer: fig. 2: paragraphs 27-29**).

With regards to claim 4, Vankka in view of Fischer teaches the modulator according to claim 3.

Vankka further teaches the modulator with

means for filling digital zeros (**fig. 1: MUX**) into the pulse shaping filter (**fig. 1: ramp generator, power level controller, and pulse shaping filters**) of the I/Q modulated signal.

Vankka is silent with respect to teaching the means for generating the step-off response followed by the step-on response of the pulse shaping filter during the guard interval such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots.

Fischer teaches an I/Q transmitter and modulator with

means for generating the step-off response followed by the step-on response of the pulse shaping filter during the guard interval (**disclosed in claim 3 and claim 9**)

such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots (**disclosed in claim 3 and claim 9**).

Therefore it would be obvious to combine the I/Q modulator means for filling digital zeros into the pulse shaping filter (**Vankka: fig. 1: ramp generator, power level controller, and pulse shaping filter**s) of Vankka with the step-off response followed by a step-on response of Fischer in order to create an enhanced transmission system which reduces the mean power loss in a system using different modulation methods, such as GMSK and 8PSK (**Fischer: paragraphs 6 and 8**) and provide a smooth transition in the guard periods between successive time slots when switching between different modulation schemes (**Fischer: fig. 2: paragraphs 27-29**).

With regards to claim 6, Vankka further teaches a modulator in accordance with claim 1, wherein

the modulator is a GMSK modulator and a 8PSK modulator (**Table 2: Abstract and Section 2: paragraph 1**).

With regards to claim 11, Vankka in view of Fischer teaches the modulator of claim 1.

Vankka teaches a modulator circuit (**fig. 1**).

Vankka is silent with respect to teaching a transmitter comprising a modulator.

Fischer teaches a transmitter comprising a modulator (**fig. 1: element 10: paragraph 3**).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the I/Q modulation circuit of Vankka with the I/Q transmitter including the I/Q modulator of Fischer in order to create an enhanced transmission system which reduces the mean power loss in a system using different modulation methods, such as GMSK and 8PSK (**Fischer: paragraphs 6 and 8**).

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vankka (A GSM/EDGE/WCMDA Modulator With On-Chip D/A Converter for Base Stations) in view of Fischer (US 2003/0160654) as applied to claim 1 above, and further in view of Khoini-Poorfard (USPN 6865235).

With regards to claim 5, Vankka in view of Fishcer teach the modulator according to claim 3.

Vankka teaches a GMSK modulator (**fig. 1 and Table 1**) and multiplexer (**fig. 1: MUX**), wherein

the multiplexer feeds complex zeros (**fig. 1: Multiplexers' inputs: Section 7**) to the pulse shaping filter (**disclosed in claim 3 and claim 9**).

Vankka is silent with respect to teaching two limitations: (item 1) a GMSK modulator with a linear branch and a quadratic branch, (item 2) a dip is generated comprising the step-off response followed by the step-on response of the pulse shaping filter such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots.

regarding (item 1) above:

(1) Fischer teaches a GMSK transmission circuit (**fig. 1: paragraphs 27-29**) and modulator (**fig. 1: paragraph 27-29**) such that

means for generating the step-off response followed by the step-on response of the pulse shaping filter during the guard interval (**disclosed in claim 3 and claim 9**)

such that the dip is introduced in the envelope of the digital I/Q signal in the guard interval between adjacent time-slots (**disclosed in claim 3 and claim 9**).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the modulation circuit including the ramp generator, power level controller, and pulse shaping filters of Vankka with the GSMK transmitter including pulse shaping filter with the mean for generating a step-off response followed

by a step-on response of Fischer in order to create an enhanced transmission system which reduces the mean power loss in a system using different modulation methods, such as GMSK and 8PSK (**Fischer: paragraphs 6 and 8**) and provide a smooth transition in the guard periods between successive time slots when switching between different modulation schemes (**Fischer: fig. 2: paragraphs 27-29**).

regarding (item 2) above:

(2) Khoini-Poorfard teaches a GMSK modulator with a linear branch and a quadratic branch (**fig. 2B: col. 6, lines 17-29**).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the GMSK modulation circuit of Vankka in view of the GSMK transmission circuit of Fischer in further view of the multi-protocol modulator of Khoini-Poorfard in order to create an improved mqdulation system capable of combining two or more modulation architectures by sharing at least one functional sub-system (**Khoini-Poorfard: col. 2, lines 10-25**) and thus requiring less chip space.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vankka (A GSM/EDGE/WCMDA Modulator With On-Chip D/A Converter for Base Stations) in view of Fischer (US 2003/0160654), further in view of Madkour (2002/0085623).

With regards to claim 10, Vankka teaches a modulator chipset (**fig. 1**) which

uses GSMK, EDGE, and 8PSK (**abstract and Table 2: note that 8PSK is obviously used for EGPRS**) and performing the step of:

step a: generating a digital I/Q signal (**fig. 1: Section 2A: paragraph 2**) having a plurality of time-slots (**Section 3: paragraph 2: obviously representing TDMA**).

Vankka is silent with respect to teaching two items: (item 1) a computer program controlling the transmitter modulation apparatus and performing the claimed steps, and (item 2) **step b**: introducing a dip in an envelope of the digital I/Q signal in a guard interval between adjacent time-slots.

Regarding (item 1) above:

Fischer teaches a transmitting apparatus (**fig. 1: abstract**)

controlled by a Digital Signal Processor (DSP) control unit (**fig. 1: element 20: paragraph 24**); and performs the step of:

(b) introducing a dip in the envelope (**fig. 2: paragraphs 13 and 27-29**) of the I/Q signal (**fig. 1**) in a guard interval between adjacent time-slots (**fig. 2: paragraphs 13 and 27-29**).

Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the I/Q modulation circuit of Vankka with the I/Q transmitting apparatus of Fischer in order to create an enhanced transmission system which reduces the mean power loss in a system using different modulation methods, such as GMSK and 8PSK (**Fischer: paragraphs 6 and 8**).

Regarding (item 2) above:

Madkour teaches that DSP is capable of using a computer program (**paragraph 37**) with respect to performing to steps (a) and (b) above.

One of ordinary skill in the art would recognize the benefit of using wireless communication system which uses a DSP capable of using a computer program to increase the system's ability to switch between a plurality of modulation schemes and increase the system's ability to adapt to channel noise characteristics and thereby allow the transmitted downlink which have less errors. Therefore it would obvious to one of ordinary skill in the art at the time the invention was made to combine the I/Q modulator of Vankka in view of the I/Q transmitter and modulator of Fischer in further view of communication system of Madkour in order to create an enhanced system which increases the system's ability to adapt to channel noise characteristics and thereby allow the transmitted downlink signal to have less error and be easily corrected by interference cancellation performed at the receiver (**Madkour: paragraph 9**).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Mazur (USPN 6438115) discloses that EGPRS uses 8PSK modulation (Col. 3, lines 41-60).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Perez whose telephone number is 571-270-3231. The examiner can normally be reached on Monday through Friday: 9am to 5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JP
10/15/2007

SHUWANG LIU
SUPERVISORY PATENT EXAMINER